REMARKS

After entry of this amendment, claims 1-24 remain pending. In the present Office Action, claims 1-8 and 11-24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Pontius et al., U.S. Patent No. 6,029,243 ("Pontius"). Claims 9-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pontius in view of allegedly well known features. Applicants respectfully traverse these rejections.

Additionally, Applicants respectfully traverse the assertion that trace caches are well known (Official Notice of which is taken in the present Office Action). Applicants note that the Official Notice was also traversed in the previous Response to Office Action, and thus the traverse is seasonable. Accordingly, pursuant to MPEP 2144.03, the Examiner is required to provide adequate evidence if the rejection is to be maintained. Furthermore, even if the Examiner proves that trace caches are well known, that still would not render claim 9 obvious. For example, claim 9 recites "the prediction circuit is configured to predict the execution latency responsive to the floating point operation being included in a trace, and wherein the trace cache is configured to store an indication of the execution latency predicted by the prediction circuit". Such features are not taught by the mere existence of trace caches, nor would such features be obvious in view of Pontius and trace caches.

Section 102 Rejection

Applicants respectfully submit that each of claims 1-24 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "a scheduler configured to schedule the floating point operation for execution, wherein the prediction circuit is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution."

Pontius does not teach or suggest the above highlighted features. Rather, Pontius teaches "logic for determining when to execute a floating point operation in hardware and when to trap makes its determination as a function of a requested result precision and the

maximum apparent precision of the operands" (Pontius, col. 2, lines 30-34). Thus, Pontius teaches a system of determining the execution precision at execution time. No prediction of precision is made. For example, in Fig. 1, the trap logic TPL makes the determination based on the apparent precision of the operands and the requested result precision derived from the instruction (see, e.g., Pontius, col. 5, lines 7-10). The operands are present at the time of execution (e.g. in REGA and REGB, see Fig. 1), and the requested result precision is provided on the inputs PH and PL, again at the time of execution. See, e.g., Pontius, col. 3, lines 35-38; col. 4, lines 13-14; col. 4, lines 30-33; and col. 4, lines 57-65. Pontius is silent on how the PH and PL inputs are generated, and thus Pontius only teaches that the PH and PL inputs are provided at the time of execution.

With respect to original claim 8, the Office Action asserts that "the execution latency can be measured from any point in the processing pipeline, including upon issuance from the scheduler". Applicants do not disagree that latency may be MEASURED from any desired point. However, the features of claim 8 include "the prediction circuit is configured to PREDICT the execution latency of the floating point operation responsive to dispatch of the floating point operation to the scheduler". Similarly, measuring the execution latency from any point in the pipeline would not teach or suggest "the prediction circuit is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution."

For at least the above-stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-15, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2-15 recites additional combinations of features not taught or suggested in the cited art.

Claim 16 recites a combination of features including: "scheduling the floating point operation from a scheduler for execution in a floating point unit wherein the predicting is performed prior to the scheduling." The same teachings highlighted above with regard to claim 1 are alleged to teach the combination of features of claim 16. Applicants respectfully submit that the cited art does not teach or suggest the above

highlighted features of claim 16, either. Accordingly, Applicants respectfully submit that claim 16 is patentable over the cited art. Claims 17-24, being dependent from claim 16, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 17-24 recites additional combinations of features not taught or suggested in the cited art.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-91300/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,

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